REMARKS

Claims 1-8 were examined, and all claims arerejected. Claim 9 and 10 are added. Thus, claims 1-10 are pending.

The disclosure is objected to because page 1 of the specification includes references to patent applications without serial numbers and dates. Applicant has therefore amended the specification to include the serial numbers and dates.

Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,800,574) in view of Lowe et al. (U.S. Patent No. 6,173,243). Applicant respectfully traverses this rejection for the reasons set forth below.

The present invention is directed to a signal processing apparatus having a channel pooling signal processor 76 and a digital signal processor (DSP) 72, wherein the channel pooling signal processor 76 performs more computationally intensive signal processing operations than the DSP 72. The channel pooling signal processor 76 has computation units 36, a test interface 34 for testing the function of the computation units 36, a microprocessor 74 for managing data flow into and out of the channel pooling signal processor 76, and an interconnect mechanism 32 for connecting the computation units 36, the interface 34, and the microprocessor 74.

The applied references do not suggest the claimed channel pooling signal processor, which is a specialized processor that is reconfigurable and designed to perform intensive mathematical processing. As claimed, and as shown in Figs. 2-5, the channel pooling signal processor 76 includes computation units 36, a test interface 34, a microprocessor 74, and an interconnect mechanism 32. The computation units 36 are located within a heterogeneous reconfigurable multiprocessor 66.

While Tanaka may disclose two processors 300, 302 (see Fig. 4) operating at two different rates, neither of these processors is disclosed as being a channel pooling signal processor. In fact, there is virtually no disclosure regarding the structure of Tanaka's processors. And contrary

to the Examiner's statement in the Office Action, Tanaka's Fig. 3 does not illustrate computation units of one of the Fig. 4 processors, which the Examiner asserts teaches the claimed channel pool signal processor. Rather, Fig. 3 illustrates interfaces of the modulator 100 and demodulator 200 of Figs. 1 and 2.

Even were the Examiner correct in that Fig. 3 illustrated details of one of the processors of Fig. 4, the processors would still not be equivalent to the claimed channel pool signal processor, which includes computation units. The claimed computation units perform computationally intensive operations, such as channel decoding, equalization, chip-rate processing, synchronization, channelization, parameter estimation, etc. (See specification, page 7, lines 13-25.) In Tanaka's Fig. 3 no computation units are shown. Fig. 3 merely illustrates D/A and A/D converters and filters, which do not perform any computations; the converters merely convert signals from analog to digital or visa-versa, and the filters are passive devices that remove unwanted noise. Thus, Takana does not suggest the claimed channel pooling signal processor. Reconsideration and withdrawal o the prior art rejection is therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: December 23, 2003

Respectfully submitted,

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